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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,955	11/20/2003	Ha C. Vu	08211/0200374-US0	9020

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,955	VU, HA C.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-14* is/are rejected.

7)☒ Claim(s) *5-8 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the recited limitations "generating a divided down signal in response to the prescaler receiving the Mth input pulse"; and "generating a fast clock signal in response to the synchronized signal" in claim 15 are not supported by either by the disclosure or the drawings.

Claim Objections

2. Claims 1, 10, and 16 are objected to because of the following informalities:

Claim 1, lines 9-10, "a preset integer" should be changed to --the preset integer--;

Claim 10, line 6, "a prescaled pulse" should be changed to --the prescaled pulse--; and

Claim 16, line 3, "a prescaled pulse" should be changed to --the prescaled pulse--;

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which

it is most nearly connected, to make and/or use the invention. The claimed limitations that "generating a divided down signal in response to the prescaler receiving the Mth input pulse"; and "generating a fast clock signal in response to the synchronized signal", in claim 15, have not been enabled in the specification. The details of such functions are not seen in the description of the preferred embodiment. For example, it is unclear as how to generate a divided down signal (clkout in instant Fig.3) in response to the prescaler (310) receiving the Mth input pulse (614 in instant Fig.6), and it is also unclear as how a fast clock signal (910 in instant Fig.9) is generated in response to the synchronized signal (clock_sync in instant Fig.1). It is not clear as currently defined, how the instant invention can perform the recited functions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,603,360) in view of Hunt, Jr. et al. (US 6,385,276).

With regard to claims 1 and 10, Kim et al. discloses in Figs. 2-6 a circuit for dividing periodic input pulses by a preset integer M (K, K+1), and a method of use thereof, comprising a dual modulus prescaler (210) arranged to receive periodic input pulses (MCLK) and to count the received input pulses for generating prescaled pulses (CLKMDL); and a swallow counter (230) arranged to change the modulus control signal (C1) to a different value in response to the

prescaler receiving every Mth input pulse. The reference circuit meets all of the claimed limitations, except for the limitation that the modulus control signal (C1) is ignored at least until the onset of a next input pulse (pulse 1 or 5 of signal CNT1) is received as recited in the claim. Hunt, Jr. et al. discloses in Figs. 1-3 a dual modulus prescaler, similar to the circuit of Kim et al., having the modulus control signal (divc) is ignored; when a prescaled pulse (fb) is generated from a selected input pulse (fin); at least until the onset of a next input pulse (2^{th} pulse) of signal fin is received as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement the teaching of Hunt of ignoring the modulus control signal at least until the onset of a next input pulse in order to ensure the correctness of critical state transitions (low to high/or high to low for determining the mode of operation of the dual modulus divider).

With regard to claims 2-3 and 11-14, the references also meet the recited limitations in these claims (see Fig.3 of Hunt).

Claim 9 is similarly rejected; note the above discussion with regard to claims 1 and 10.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Hunt, Jr. et al. as applied to claims 1-3 above, and further in view of Keating (US 5,867,068).

The above discussed the circuit of the references meets all of the claimed limitations except for an OR gate (1040 in instant Fig.10) for ORing the modulus control signal (div4) with another signal. Keating teaches in Fig. 15 a prescaler includes an OR gate for ORing the modulus control signal (1520) with another signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the prescaler including OR gate taught by Keating with the prior art in order to provide a desired symmetrical frequency signal.

Allowable Subject Matter

8. Claims 5-8 and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest a circuit (300 in instant Fig.3) for dividing periodic input pulses (clkin) by a preset integer M (PLLDIV), as recited in claim 5, comprising a dual modulus prescaler (310); a swallow counter (330); and specifically the limitation directed to a program counter (320) to generate a reset signal (counter_reset) in response to the prescaler receiving the Mth input pulse, and wherein the swallow counter changes the modulus control signal (DIV4) in response to the reset signal.

The prior art of record does not disclose or suggest a method (as shown in Figs. 7-10), as recited in claim 16, a step of generating the prescaled pulses (924) includes initializing (810) a vector of state variables (D2D1D0: 111) when the prescaled pulse is generated (CK45=1), and updating (820) the vector during the next input pulse in a way that is indifferent to the updated modulus control signal (DIV4=XX).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Ooms et al. (US 4,325,031) is cited as of interest because it discloses a divider with dual modulus prescaler for phase locked loop frequency synthesizer.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and

Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
April 30, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800